

WHAT IS CLAIMED IS:

- 1 1. A metal-insulator-metal (MIM) capacitor plate, comprising:
 - 2 a first conductive layer, the first conductive layer comprising a first material;
 - 3 at least one thin conductive material layer disposed over the first conductive layer, the
 - 4 thin conductive material layer comprising a second material, the second material being different
 - 5 than the first material; and
 - 6 at least one second conductive layer disposed over at least one of the at least one thin
 - 7 conductive material layers.
- 1 2. The MIM capacitor plate according to Claim 1, wherein the at least one thin conductive
- 2 material layer comprises TiN, TaN, or WN.
- 1 3. The MIM capacitor plate according to Claim 1, wherein the at least one thin conductive
- 2 material layer comprises a thickness of about 450 Angstroms or less.
- 1 4. The MIM capacitor plate according to Claim 1, wherein the at least one thin conductive
- 2 material layer comprises:
 - 3 a first barrier layer disposed over the first conductive layer; and
 - 4 a conductive layer disposed over the first barrier layer.
- 1 5. The MIM capacitor plate according to Claim 4, wherein the first barrier layer comprises
- 2 Ti, Ta or W, and wherein the conductive layer comprises TiN, TaN, or WN.
- 1 6. The MIM capacitor plate according to Claim 4, wherein the at least one thin conductive
- 2 material layer further comprises a second barrier layer disposed over the conductive layer.

1 7. The MIM capacitor plate according to Claim 6, wherein the first barrier layer comprises
2 Ti, Ta or W, wherein the conductive layer comprises TiN, TaN, or WN, and wherein the second
3 barrier layer comprises Ti, Ta or W.

1 8. The MIM capacitor plate according to Claim 1, wherein the at least one second
2 conductive layer comprises the first material.

1 9. The MIM capacitor plate according to Claim 1, wherein the first conductive layer and the
2 at least one second conductive layer comprise Al.

1 10. The MIM capacitor plate according to Claim 1, wherein the MIM capacitor plate is
2 formed in a metallization layer of a semiconductor device, the metallization layer comprising a
3 plurality of conductive lines having a first thickness, wherein the MIM capacitor plate comprises
4 the first thickness.

1 11. The MIM capacitor plate according to Claim 1, wherein the MIM capacitor plate
2 comprises a bottom plate of a MIM capacitor.

1 12. The MIM capacitor plate according to Claim 1, wherein the MIM capacitor plate
2 comprises a top plate of a MIM capacitor.

1 13. A metal-insulator-metal (MIM) capacitor, comprising:
2 a first plate;
3 a dielectric material disposed over the first plate; and
4 a second plate disposed over the dielectric material, wherein the first plate or the second
5 plate comprises:

6 a first conductive layer, the first conductive layer comprising a first
7 material;
8 at least one thin conductive material layer disposed over the first conductive layer,
9 the at least one thin conductive material layer comprising a second material, the second
10 material being different than the first material; and
11 at least one second conductive layer disposed over at least one of the at least one
12 thin conductive material layers.

1 14. The MIM capacitor according to Claim 13, wherein either the first plate or second plate is
2 formed in a metallization layer of a semiconductor device, the metallization layer comprising a
3 plurality of conductive lines having a first thickness, wherein the MIM capacitor first plate or
4 second plate comprises the first thickness.

1 15. The MIM capacitor according to Claim 13, wherein the at least one thin conductive
2 material layer comprises TiN, TaN, or WN.

1 16. The MIM capacitor according to Claim 15, wherein the at least one thin conductive
2 material layer comprises a thickness of about 450 Angstroms or less.

1 17. The MIM capacitor according to Claim 13, wherein the at least one thin conductive
2 material layer comprises:

3 a first barrier layer disposed over the first conductive layer; and
4 a conductive layer disposed over the first barrier layer.

1 18. The MIM capacitor according to Claim 17, wherein the first barrier layer comprises Ti,
2 Ta or W, and wherein the conductive layer comprises TiN, TaN, or WN.

1 19. The MIM capacitor according to Claim 17, wherein the at least one thin conductive
2 material layer further comprises a second barrier layer disposed over the conductive layer.

1 20. The MIM capacitor according to Claim 19, wherein the first barrier layer comprises Ti,
2 Ta or W, wherein the conductive layer comprises TiN, TaN, or WN, and wherein the second
3 barrier layer comprises Ti, Ta or W.

1 21. The MIM capacitor according to Claim 13, wherein the first conductive layer and the at
2 least one second conductive layer comprise the same material.

1 22. The MIM capacitor according to Claim 13, wherein the first conductive layer and the at
2 least one second conductive layer comprise Al.

1 23. The MIM capacitor according to Claim 13, wherein the first plate comprises:
2 a first conductive layer, the first conductive layer comprising a first material;
3 at least one first thin conductive material layer disposed over the first conductive layer,
4 the at least one first thin conductive material layer comprising a second material, the second
5 material being different than the first material; and
6 at least one second conductive layer disposed over at least one of the at least one thin
7 conductive material layers;
8 and wherein the second plate comprises:
9 a third conductive layer disposed over the dielectric material, the third conductive
10 layer comprising a third material;
11 at least one second thin conductive material layer disposed over the third
12 conductive layer, the at least one second thin conductive material layer comprising a fourth
13 material, the fourth material being different than the third material; and
14 at least one fourth conductive layer disposed over at least one of the at least one
15 second thin conductive material layers.

1 24. The MIM capacitor according to Claim 23, wherein the first conductive layer, the at least
2 one second conductive layer, the third conductive layer and the at least one fourth conductive
3 layer comprise Al, and wherein the at least one first thin conductive material layer and the at
4 least one second thin conductive material layer comprise about 450 Angstroms or less of TiN,
5 TaN, or WN.

1 25. The MIM capacitor according to Claim 24, wherein the at least one first thin conductive
2 material layer and the at least one second thin conductive material layer further comprise a
3 barrier layer disposed over or under the TiN, TaN or WN.

- 1 26. A semiconductor device, comprising:
2 a workpiece;
3 at least one metallization layer formed over the workpiece;
4 at least one metal-insulator-metal (MIM) capacitor formed over the workpiece, the MIM
5 capacitor comprising a first plate formed within the at least one metallization layer, a dielectric
6 material disposed over the first plate, and a second plate disposed over the dielectric material;
7 and
8 at least one first conductive line formed in the at least one metallization layer of the
9 semiconductor device, wherein the at least one first conductive line comprises a first thickness,
10 and wherein the MIM capacitor first plate comprises the first thickness.
- 1 27. The semiconductor device according to Claim 26, wherein the first plate and the at least
2 one first conductive line comprise:
3 a first conductive layer, the first conductive layer comprising a first material;
4 at least one thin conductive material layer disposed over the first conductive layer, the
5 thin conductive material layer comprising a second material, the second material being different
6 than the first material; and
7 at least one second conductive layer disposed over at least one of the at least one thin
8 conductive material layers.
- 1 28. The semiconductor device according to Claim 27, wherein the first conductive layer and
2 the at least one second conductive layer comprise Al, and wherein the at least one thin
3 conductive material layer comprises TiN, TaN, or WN.

1 29. The semiconductor device according to Claim 27, wherein the at least one thin
2 conductive material layer comprises a first layer of Ti, Ta or W disposed over the first
3 conductive layer, and a second layer of TiN, TaN, or WN disposed over the first layer of Ti, Ta
4 or W.

1 30. The semiconductor device according to Claim 27, wherein the at least one thin
2 conductive material layer comprises a third layer of Ti, Ta or W disposed over the second layer
3 of TiN, TaN, or WN.

1 31. The semiconductor device according to Claim 26, wherein the first plate is electrically
2 coupled to at least one first conductive line in the metallization layer.

1 32. A method of manufacturing a metal-insulator-metal (MIM) capacitor, the method
2 comprising:

3 providing a workpiece;

4 depositing a first conductive layer over the workpiece, the first conductive layer
5 comprising a first material;

6 depositing at least one thin conductive material layer over the first conductive layer, the
7 at least one thin conductive material layer comprising a second material, the second material
8 being different than the first material;

9 depositing at least one second conductive layer over at least one of the at least one thin
10 conductive material layers; and

11 patterning the at least one second conductive layer, the at least one thin conductive
12 material layer and the first conductive layer to form a first plate.

1 33. The method according to Claim 32, further comprising forming a plurality of conductive
2 lines in the at least one second conductive layer, the at least one thin conductive material layer
3 and the first conductive layer simultaneously while forming the first plate, wherein the plurality
4 of conductive lines resides in a metallization layer of a semiconductor device.

1 34. The method according to Claim 33, wherein patterning the at least one second conductive
2 layer, the at least one thin conductive material layer and the first conductive layer to form the
3 first plate and the plurality of conductive lines comprises using a single mask.

1 35. The method according to Claim 32, further comprising:
2 depositing a dielectric material over the first plate;
3 depositing a third conductive layer over the dielectric material; and
4 patterning the third conductive layer and the dielectric material to form a MIM capacitor,
5 wherein the patterned third conductive layer comprises a top plate of the MIM capacitor, and
6 wherein the dielectric material comprises a capacitor dielectric of the MIM capacitor.

1 36. The method according to Claim 32, further comprising, before depositing the first
2 conductive layer over the workpiece:
3 forming a second plate over the workpiece, the second plate comprising a bottom plate of
4 a MIM capacitor; and
5 forming a capacitor dielectric over the second plate, wherein the first plate comprises a
6 top plate of the MIM capacitor, and wherein depositing the first conductive layer comprises
7 depositing the first conductive layer over the MIM capacitor.

1 37. The method according to Claim 32, wherein depositing the at least one thin conductive
2 material layer comprises depositing about 450 Angstroms of material.

1 38. The method according to Claim 32, wherein depositing the at least one thin conductive
2 material layer comprises depositing TiN, TaN, or WN.

1 39. The method according to Claim 38, further comprising depositing a barrier layer of Ti,
2 Ta, or W over or beneath the TiN, TaN, or WN.

1 40. The method according to Claim 32, wherein depositing the first conductive layer and
2 depositing the at least one second conductive layer comprise depositing Al.